Execution Model: Neuromorphic Computation

Seminarbericht

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Abstract

Neuromorphic computation is the concept, developed by Carver Mead in the late 1980s, of using very large scale integrated circuits to mimic the behaviour of synapses and neurons occurring in neural systems. After an introduction to neuromorphic computation in general, this report presents the limitations of traditional computing considering the efficiency of simulated neural systems. To illustrate those limits a comparison between the benchmark results of a neural simulation running on the currently 4th highest performing super computer "K" in Kobe, Japan and the human brain as the biological counterpart will be drawn. In the last decade, many teams and organizations have made major advances researching and developing neuromorphic systems. In this report, the three designs SpiNNaker, Spikey (both from the Human Brain Project) and TrueNorth (System of Neuromorphic Adaptive Plastic Scalable Electronics) will be discussed and compared to each other, as well as the previously addressed computer "K" and the human brain. The different hardware choices, implementations and resulting preferences of those systems allow for an in-depth analysis of individual perks and promises. Furthermore, the prospects and benefits of the recently prototyped memory resistor in general computing and its consequences for neuromorphic systems will be debated. Finally, possible near and far future applications of neuromorphic computation will be addressed.

Contents

1. Introduction **4**
1.1. The Human Brain 4
1.2. Goals of Neuromorphic Computation 4

2. Benefits **5**
2.1. High Performance Computer "K" 5
2.2. Comparison between "K" and the Human Brain 6

3. State of the Art **7**
3.1. General Device Concept 7
3.2. SpiNNaker 8
3.3. Spikey 10
3.4. Truenorth 11
3.5. Final Comparison 12

4. Upcoming Technologies **13**
4.1. The Memory Resistor 13
4.2. Hewlett Packards "The Machine" 13
4.3. Memristors in Neuromorphic Computation 14

5. Conclusion **16**
5.1. Applications of Neuromorphic Computation 16
5.2. Final Words 17

Bibliography **18**

Appendices **21**

A. Memristor - The missing element **22**

B. Titanium Dioxide Memristor **23**

List of Figures **24**

List of Tables **25**

1. Introduction

1.1. The Human Brain

Neuromorphic computation describes a computing concept inspired by the structure and function of biological neural systems. To get qualitative results which determine the efficiencies of such computational approaches, neuromorphic systems can be compared to natural ones, such as the human central nervous system. It is the most complex neural system nature produced through evolution and because of the fact that such a system can exist, it should theoretically be possible to artificially recreate it (even if that means to rebuild a human brain in the ever lavish process of putting it together out of single atoms). The human brain is a network of roughly 85 billion neurons in which each neuron is linked to up to 10 thousand others. Thus, to establish a connection between any two neurons within this network, merely 2 to 3 intermediate neurons might be needed, at most. A single neuron represents a processing unit, calculating its output up to 1 thousand times per second, but typically about 300 times per second. Taken together, the human brain could be seen as a massive parallel computing device with 85 billion cores running at very slow frequencies - in comparison to traditional CPUs. Overall the human brain has a performance of up to 1 petaFLOPS with a remarkably low energy consumption of 20 Watt, analogous to that of a dim light bulb. [Jam12] [Luk] [Den89] [J+01]

1.2. Goals of Neuromorphic Computation

The goals of neuromorphic computation are efficiencies like those of the human brain in terms of processing power, storage capacity and energy consumption. Currently efficiencies of traditional computers are many orders of magnitude worse with Moore's Law slowly coming to a halt. Besides many practical applications where brain-inspired information processing promises much better results, neuromorphic researchers also hope to learn a lot in the process of studying and essentially recreating neural systems. [Chr99]

2. Benefits

2.1. High Performance Computer "K"

Another illustration of performance differences between the human brain and traditional computers is the biggest neural simulation to date which was run on the computer "K" by RIKEN HPCI Program for Computational Life Sciences, the Okinawa Institute of Technology Graduate University in Japan and the Forschungszentrum Jülich in Germany. "K" as the currently 4th most powerful high performance computer has the raw specifications as seen in Table 2.1. The simulation consisting of 1.73 billion neurons connected by 10.4 trillion synapses represents about 1% of the human brain. Nevertheless it took "K" 40 minutes to calculate only 1 second of brain activity consuming ~8,500 kilowatt hours and using about 1 petabyte of memory. [Ins13]

Peak Performance	~11.3 PetaFLOPS
Power Consumption	~12.7 Megawatt
Memory	~1.5 Petabyte

Table 2.1.: "K" specifications [TOP15]

2.2. Comparison between "K" and the Human Brain

Separating efficiencies in terms of speed, energy consumption and storage usage, the differences of "K" and the human brain are immense. Assuming linear scaling, the time it would take "K" to simulate 100% of brain activity would be 66 hours and 40 minutes. Thus, the performance of "K" which is 10 times larger than the brain's performance is not reflected in the computing time. There seem to be a lot more overhead and/or bottlenecks when trying to simulate brain activity with traditional computers. In fact the human brain is about 240,000 times faster than "K" regarding the processing of neural signals.

Examining the energy consumption of "K" in contrast to that of the human brain results in an even bigger factorial gap. Scaling up "K" so it is able to simulate 100% of brain activity in real time would result in an energy consumption of 8,500 kilowatt hours (due to the simulation running only one second instead of 40 minutes). The human brain only consumes about 6 milliwatt hours in one second of activity rendering it about 1.4 billion times more energy efficient than "K".

In terms of storage capacity, "K" and the human brain are barely comparable. A widespread theory about how the brain stores memories and data is through the constant activation of synapses. Assuming each synapse is either activated or deactivated representing a binary digit, the human brain would have a capacity of 50 terabytes due to the presence of about 400 trillion synapses. However, due to synaptic plasticity such an analogy between synapses and storage capacity of the brain seems unlikely. Estimates based on this principle are ranging from 100 terabytes to 5 petabytes. Nevertheless even 100 terabytes in the volume of a human brain would be quite impressive given today's standards; especially considering that the brain performs a variety of other tasks in addition to storing data. [Pau10]

Taken together, the human brain remains by far superior even compared to the 4th highest performing computer to date. Utilizing even a fraction of what should be possible by mimicking human brain systems could result in major efficiency gains for computation in general.

3. State of the Art

3.1. General Device Concept

Neuromorphic systems differ widely from concept to concept due to non-standardized approaches for chip internal signal processing resulting in diverse traits and preferences. A neuromorphic chip in general can use digital or analog circuits. It typically consists of an array of processor cores, a chip interface, an asynchronous package routing system with fault tolerant relay capabilities and occasional architecture specific parts. Each processor core simulates/emulates one or more neurons, collecting input signals and computing outputs on demand. In addition to eliminating the Von-Neumann-Bottleneck, this asynchronous calculation behaviour results in a much higher energy efficiency than traditional computation. The core only works when signals are received and is essentially off when it registers no input lacking any kind of idle process. The chip interface is responsible for inter-chip-communication enabling the possibility of scalable systems as well as communication with circuitry the chip is integrated in. The asynchronous package routing system consists of the Network on Chip (NoC) and the router, connecting cores and doing the conveying part of the purpose synapses fulfill in biological neural systems. In contrast to a living brain the routing system is not responsible for weakening or strengthening signals in terms of synaptic plasticity. All modeling of this plasticity is done in the cores of the chip. Nevertheless the fault tolerant property in neuromorphic routing systems is something inspired by neural systems. As material faults in the chip hardware can threaten to render the whole system useless, preventive measures are needed. The human brain is constantly replacing neurons and delegating their workload to other neurons. An analogous method widespread in neuromorphic computing is the relaying around broken neurons in which the system registers them and assigns their workload to others. As values for synaptic plasticity are stored in the chip's RAM they can be accessed by functioning neurons to assimilate the behaviour of broken ones.

This description served as a broad framework of how neuromorphic chips in general are structured and how their basic behaviour and cooperation lead to a brain-like processor. Going into more detail considering each part of a neuromorphic chip at this point would go beyond the scope of this report. Instead a comparison between recent neuromorphic designs of different working groups follows.

3.2. SpiNNaker

SpiNNaker (Spiking Neural Network Architecture) is a neuromorphic chip design by the Human Brain Project. Due to currently superior manufacturing processes the development team settled for an entirely digital approach, using 18 ARM9 processors on a die area of $102mm^2$. A first prototype has been finished in 2009 and the first fully operational chips have been delivered in 2011. A concept of the whole chip can be seen in figure 3.1.

The final SpiNNaker machine consists of about 60 thousand chips with 1 million processor cores altogether. It is capable of simulating about 1 billion neurons and 1 trillion synapses while consuming 50 Kilowatt on average. With this capability SpiNNaker would be able to run the simulation of "K" in real time while using only a fraction of the energy required. Even though this is a large step forwards from traditional computing, a major efficiency gap remains considering the low energy consumption and the volumetric size of biological networks. The SpiNNaker-machine still needs several racks filled with equipment and neuromorphic microchips to perform as it does. [Adv12a] [Ste14]

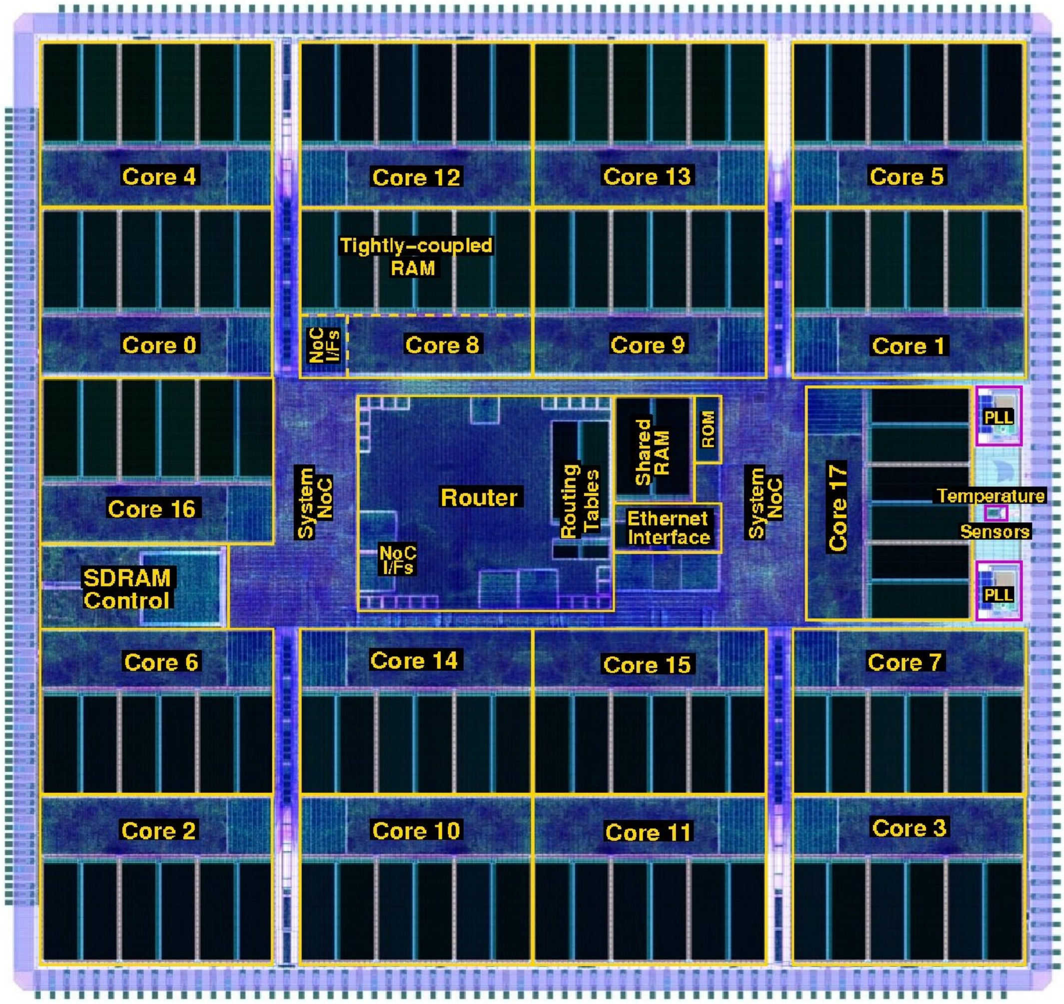

Figure 3.1.: Concept SpiNNaker Chip [Adv12b]

3.3. Spikey

In contrast to SpiNNaker, Spikey is realized using analog neurons and synapses. Compared to SpiNNaker's simulation capabilities the Spikey chip's raw neuron count is very limited with 382 neurons, each having 256 synapses. Yet, Spikey makes up for it with a 10 to 100 thousands times higher firing frequency of each neuron compared to biological systems. This allows the system to emulate more neurons than it actually consists of. Furthermore Spikey's analog approach arguably results in a more suitable model of biological neural systems. Discreet synapse weights and other variables used for processing are instead represented by the whole continuum of possible values which makes the entire system more precise compared to digital ones. A mayor drawback however is the before mentioned inferior manufacturing process of analog circuits which results in worse miniaturization and by association performance.

Taken together Spikey is a very interesting neuromorphic chip based on a more natural, analog approach with mayor differences compared to SpiNNaker. As analog circuit manufacturing improves, such chips could soon outperform digital ones, especially with the use of memory resistors, which were not used by the Spikey system. [And07]

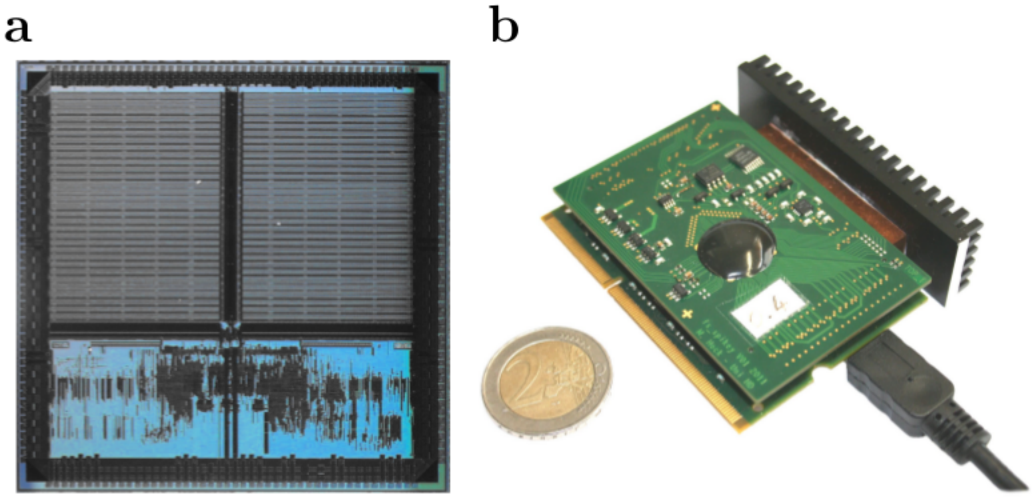

Figure 3.2.: Spikey chip (a) and system with chip under sealing (b) [T$^+$15]

3.4. Truenorth

As the most modern concept of the three presented, the development of the TrueNorth chip by the SyNAPSE-Team (Systems of Neuromorphic Adaptive Plastic Scalable Electronics) was a collaboration of IBM and several US universities. The chip is able to simulate 1 million neurons with 256 synapses each while consuming less than 70 milliwatt. Its entirely digital circuitry consists of a 64 times 64 array to a total of 4096 cores residing on a die area of approximately 150mm^2.

Systems consisting of 16 interconnected chips already have been built resulting in a network of 16 million neurons and 4 billion synapses. Plans to construct a machine out of 4 thousand chips leading to the processing power of about 5% of the human brain while consuming 4 kilowatt are currently realized. Compared to SpiNNaker this again would be a major step with a 50 fold energy efficiency gain. Yet, the human brain remains about 4 million times more efficient compared to an up scaled system of TrueNorth chips, assuming linear scaling of energy consumption and performance. [P$^+$14]

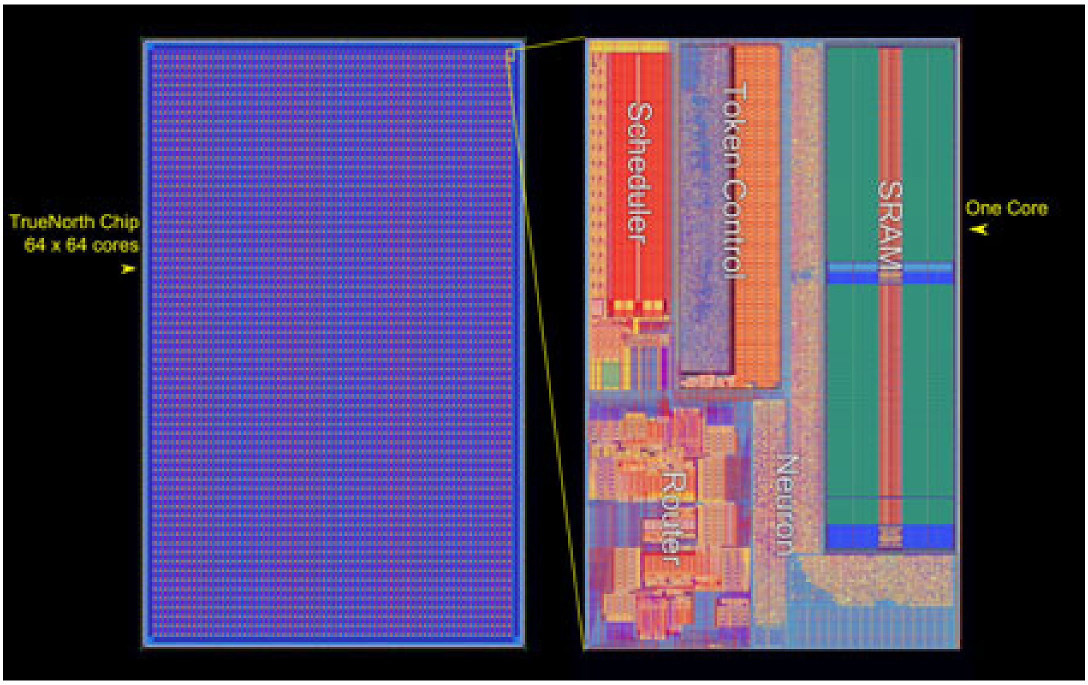

Figure 3.3.: TrueNorth Chip Core Array [Dha14]

3.5. Final Comparison

The three presented architectures were chosen to convey the differences and similarities of current neuromorphic systems. Especially Spikey, with its analog approach, stands out and shows a different but promising path of research and development. SpiNNaker and TrueNorth are more similar, with the major difference being the modularity of TrueNorth. Instead of a system wide router and network on chip for inter-core communication, TrueNorth pursues the paradigm that each core acts as an independent entity, communicating with other cores trough its own interface. Of course the technological level of SpiNNaker and TrueNorth also represents a big difference which could be due to better funding and the use of more advanced fundamental circuitry of the more modern TrueNorth chip. The comparison of the TrueNorth and SpiNNaker chips allow for a first progression estimate of digital approaches in neuromorphic computing. Table 3.1 shows the efficiencies of "K", SpiNNaker, TrueNorth and the human brain in percentage of human brain efficiency. The systems are scaled up to match the processing power of the human brain, again assuming a linear raise in energy consupmtion and processing power.

System	Efficiency (% of human brain)
HP Computer K	$\approx 7.14 * 10^{-8}$
SpiNNaker	$\approx 5 * 10^{-6}$
TrueNorth	$\approx 2.5 * 10^{-5}$
Human Brain	100

Table 3.1.: Efficiency comparison of scaled up systems

4. Upcoming Technologies

4.1. The Memory Resistor

As a very young concept, neuromorphic computing is subject to major breakthroughs and accomplishments. One of those breakthroughs is the discovery and prototyping of the memory resistor in 2008. The memory resistor (or memristor) is the last fundamental circuit element next to the Inductor, the Capacitor and the Resistor with applications in both traditional as well as neuromorphic computation. It relates the flux (time integral of voltage) to the passing charge. This means the more it is used, the lesser its resistance gets or equivalently the more charge can pass it. Its resistance can be raised again by reversing the current. In addition, as its name suggests, it remembers its resistance even when there is no applied current (non-volatile). [oTT10] [Par13]

4.2. Hewlett Packards "The Machine"

Hewlett Packard actively researches and develops the memristor with plans to build "The Machine"; a revolutionary traditional high performance computer using memristors on many occasions instead of the usually used transistors. HP asserts that the "The Machine" will be able to do 160 giga updates per second while consuming 160 kilowatt. In comparison "K" uses about 12.6 thousand kilowatt while being able to do 28.8 giga updates per second. HP even goes as far as suggesting "The Machine" for the new generation of exascale computing. Even if HPs claims are very optimistic, considering the many possibilities to integrate them in existing architectures, i.e. for non-volatile faster RAM, ALUs, CPUs etc, memristors impact for traditional computing will be immense. [Har14]

4.3. Memristors in Neuromorphic Computation

Even more impressive is the possible gain from memristors in neuromorphic computation. Concentrating on its preferences, it is apparent that memristors essentially are modeling synapses of biological neural systems. Even with the current relatively young manufacturing technology, memristors can be realized as cubes of only 3 nanometer side length. Thus, their dynamic resistance and the proportional relation between heavy usage and a strong connection is the most natural, miniature emulation of synaptic plasticity. Instead of the digital approach of using hundreds of transistors as in the architectures of TrueNorth or SpiNNaker - whereas each single transistor is as big as multiple memristors - a single memristor could be used to simulate one synapse. Even sophisticated analog systems like Spikey will most likely not be able to miniaturize as far as compressing the required circuitry of one synapse into a cube of 3 nanometer side length without the use of memristors.

Memristors are a lot faster, smaller and more energy efficient than transistors used in neuromorphic computing. Those three traits in conjunction lead to an enormous potential. Current circuit designs using memristors consist of so called cross nets. A cross net is basically a two layer high array of nanowires running vertically on one and horizontally on the other layer with memristors on each intersection. The memristors of a cross net can be dynamically configured by changing their resistances to perform different task. For example that of a half adder as shown in figure 4.1 [Kon11]. With many cross nets joined together, it is possible to model entire neurons with their respective synaptic connections. One such design can be seen in figure 4.2. Analog neuromorphic systems which use memristors in the form of crossnets are currently developed. A team of the University of California, Santa Barbara managed to produce a 100 neuron neuromorphic system with the use of memristors which is already able to conduct simple image recognition tasks. Scaling up and optimizing such a system will arguably result in a far more advanced and efficient neuromorphic computer than there are today. In theory such systems have the potential of not only approaching the performance of the human brain but even to outrun it. This is a consequence of a higher possible neuron density and the higher processing rate of memristive neuromorphic computers compared to biological neural systems. Energy consumption of such systems would still be higher but completely manageable. [Mic15]

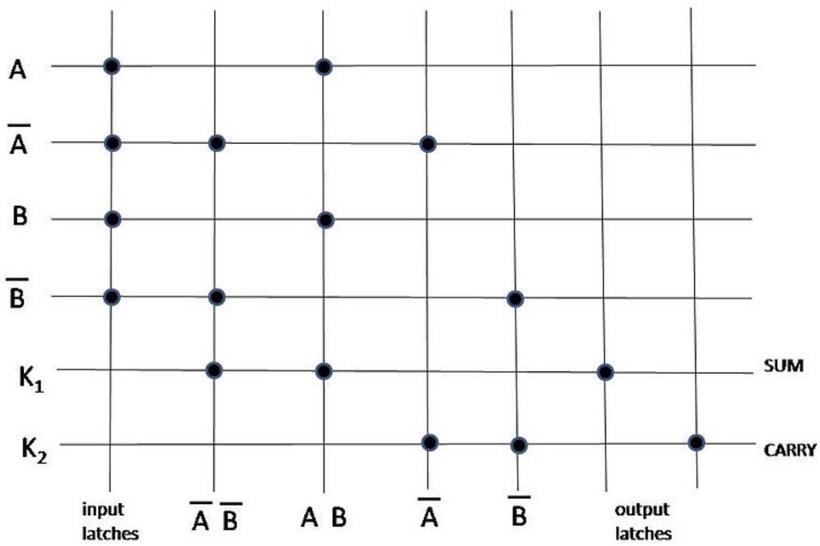

Figure 4.1.: Cross net configured as a half adder [Blm08]

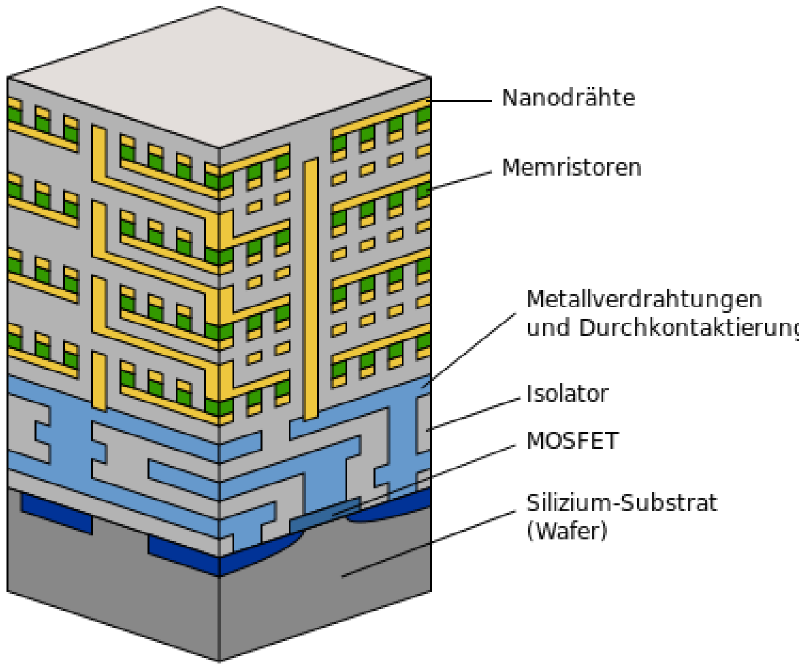

Figure 4.2.: Concept of a "Neuristor" [Mov14]

5. Conclusion

5.1. Applications of Neuromorphic Computation

The following incomplete list shows possible applications for neuromorphic computation. The list is ordered from top to bottom, upper entries represent upcoming applications in the near future while applications further down should not be expected in the next 20 years. The far future applications require more understanding and research, mostly in the subjects neuromorphic computation - as an interdisciplinary concept - depends on i.e. neuropsychology, informatics, engineering etc.

- Face, Speech, Object recognition
- Robotic terrain maneuvering
- Language interpretation
- Further extension of Moore's Law
- Understanding of the human brain
- Brain prosthetics for neurodegenerative diseases

[1]

[1] The order of this lists represents an educated guess after exposition to this topic and by no means a guarantee of the actual order of upcoming applications.

5.2. Final Words

As a very young interdisciplinary concept, neuromorphic computation is subject to rapid progression and development. In the last decade, many working groups and organizations have developed different designs and implementations, all with the goal of creating the best possible model to do brain like processing of information.

With the discovery and implementation of the memristor, more fundamental understanding of the human brain, architectural improvements and other accountable factors it is reasonable to say that the performance/efficiency of neuromorphic systems is subject to Moore's Law. Even with the most pessimistic of views on the topic major breakthroughs can be expected in no more than 15 years.

The human brain as the epitome of biological information processing remains the inspiration for artificial neural systems. As the founder of neuromorphic computation said:

"As engineers, we would be foolish to ignore
the lessons of a billion years of evolution."
– Carver Mead, 1993

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Appendices

A. Memristor - The missing element

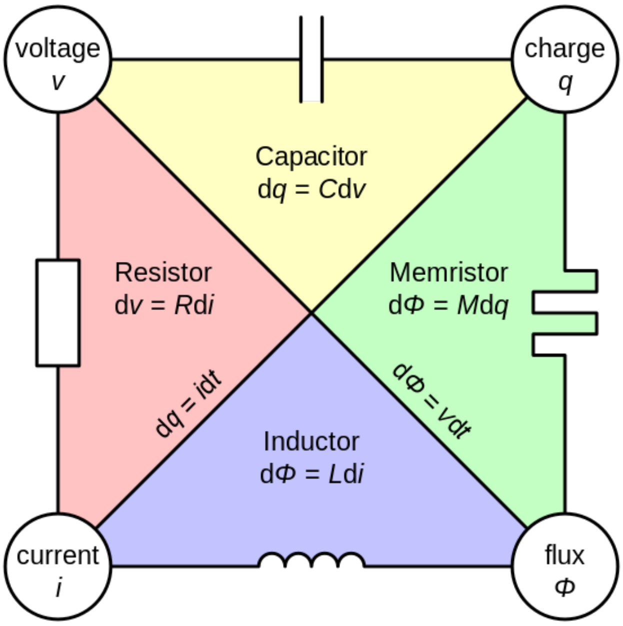

Figure A.1.: The four fundamental electric variables and circuit elements [Par13]

B. Titanium Dioxide Memristor

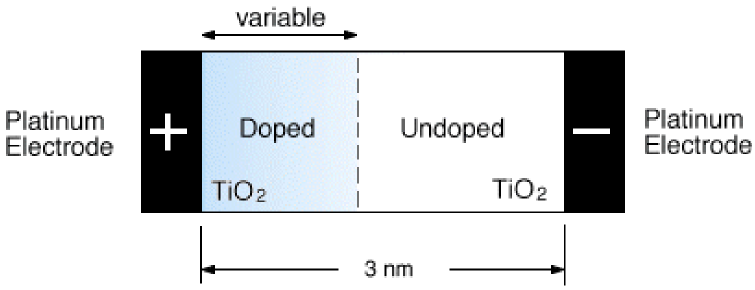

Figure B.1.: Titanium Dioxide Memristor [Jim10]

List of Figures

3.1. Concept SpiNNaker Chip [Adv12b] 9
3.2. Spikey chip (a) and system with chip under sealing (b) [T^+15] 10
3.3. TrueNorth Chip Core Array [Dha14] 11

4.1. Cross net configured as a half adder [Blm08] 15
4.2. Concept of a "Neuristor" [Mov14] 15

A.1. The four fundamental electric variables and circuit elements [Par13] . . . 22

B.1. Titanium Dioxide Memristor [Jim10] 23

List of Tables

2.1. "K" specifications [TOP15] 5
3.1. Efficiency comparison of scaled up systems 12

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